Digitization at Feed Through R&D (2) Digitizer Performance Evaluation

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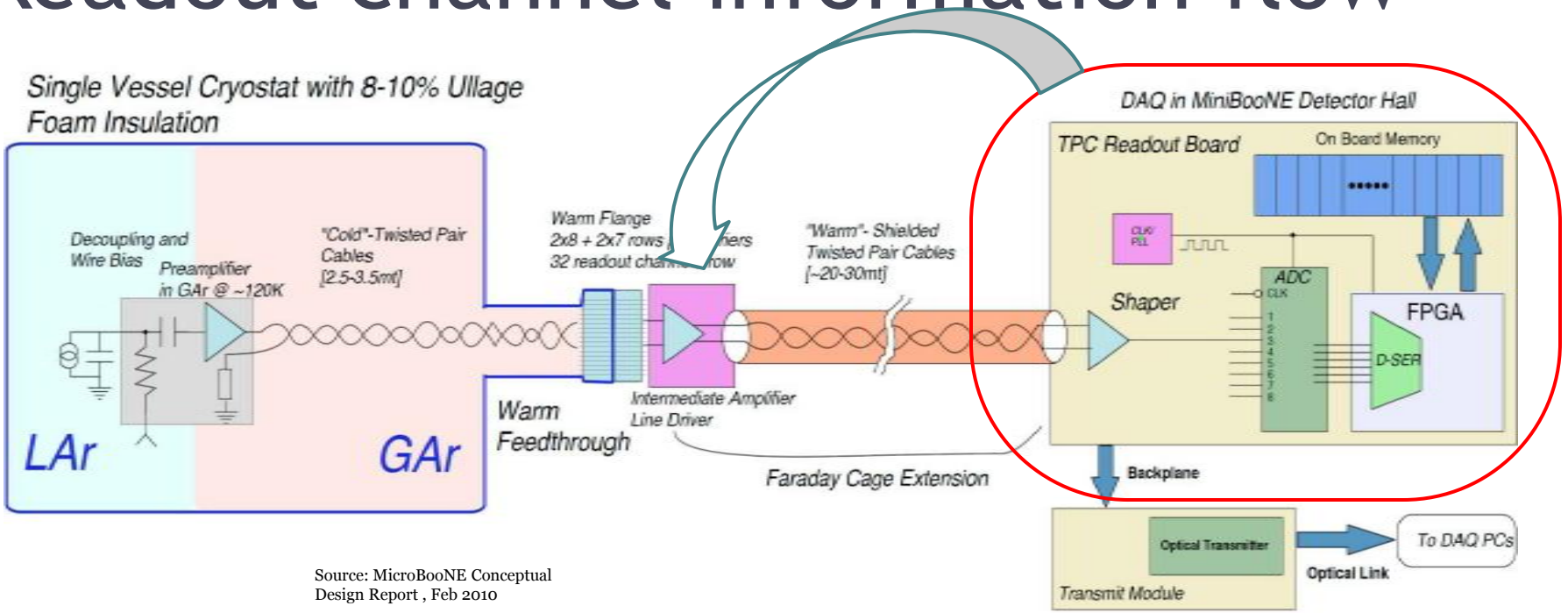
Outline

- The need for changing digitization design
- Digitization at Feed through
- The TDC FPGA Design
- Performance Tests and Results
- Conclusions

Readout channel information flow



Source: MicroBooNE Conceptual Design Report , Feb 2010

<u>Short Falls of current Design</u>

- Poor Noise Handing
- Limited cable Run

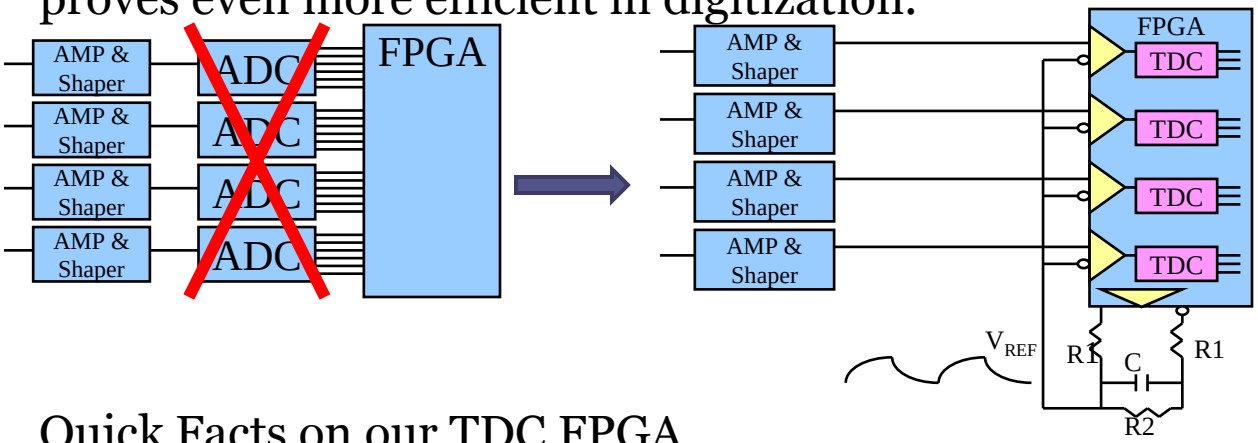
Digitization at Feed Through

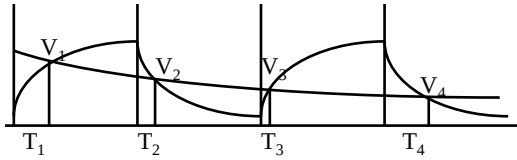
- The goal is to digitize the analog signals before they are contaminated by noise.
- However, digitization processes create noise that may contaminate signals.
- Therefore, it is a natural to minimize digital activities in the digitization processes.
- Q: How many bit transitions are considered to be minimal?

  A: 1 bit transition/data sample.

Single Slope TDC

The current design consist of ADC feeding digitized data to the FPGA for analysis. But we can Implement a TDC on an FPGA. This allows us to directly feed analog signals to the FPGA, eliminating extra ADC hardware. This scheme proves even more efficient in digitization.



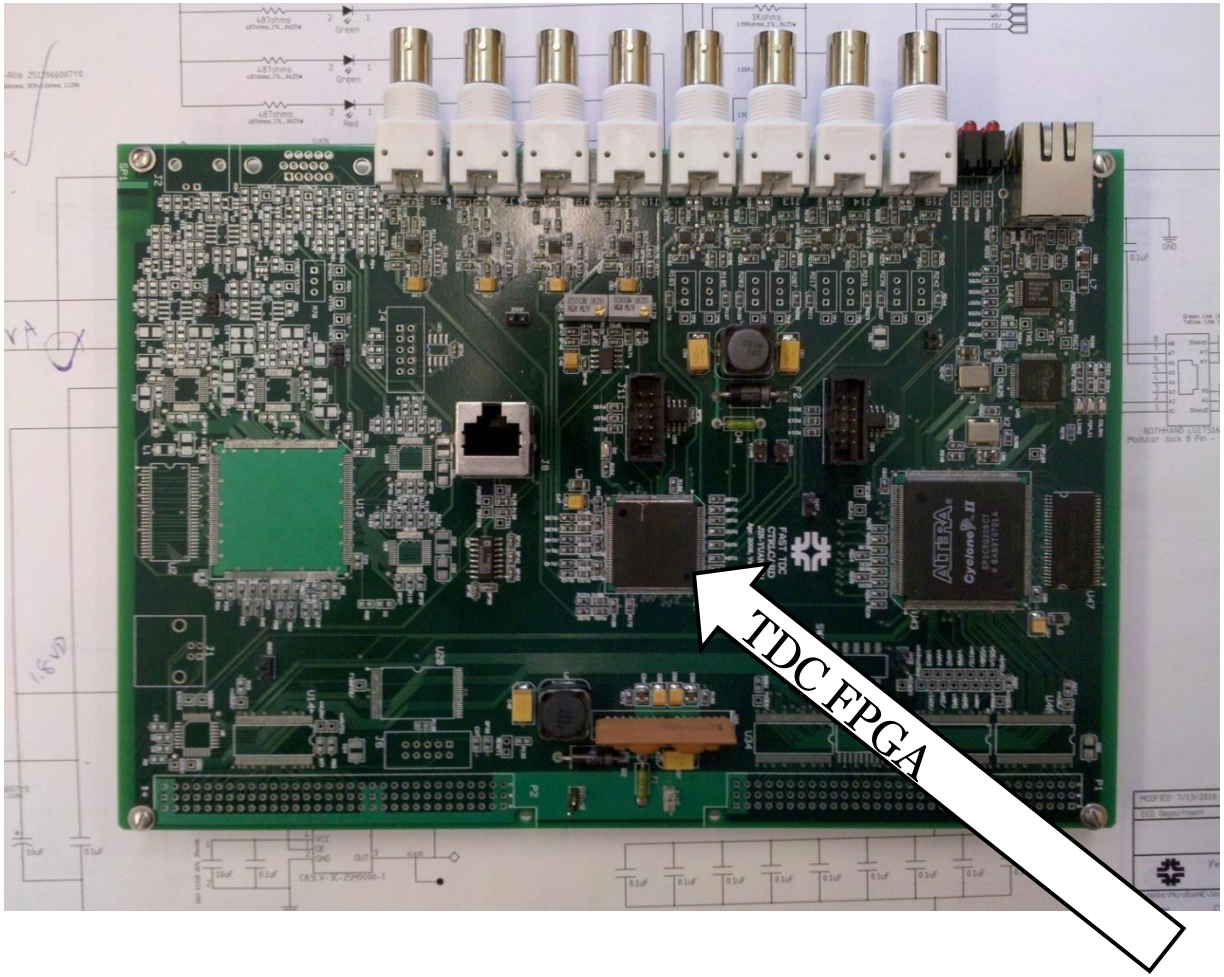


RC circuit creates Ramping reference voltage, which is compared with analog signals in FPGA. Hit time is measured to a high precision. Signals can be reconstructed using the hit times.

<u>Quick Facts on our TDC FPGA</u>

- Implemented on Altera Cyclone FPGA
- Primary firmware employs delay chains to determine transition time
- Wave Union launcher is implemented to ameliorate ultra wide bins effect
- TDC can run to a precision of 70 ps (LSB)

Fast TDC Card

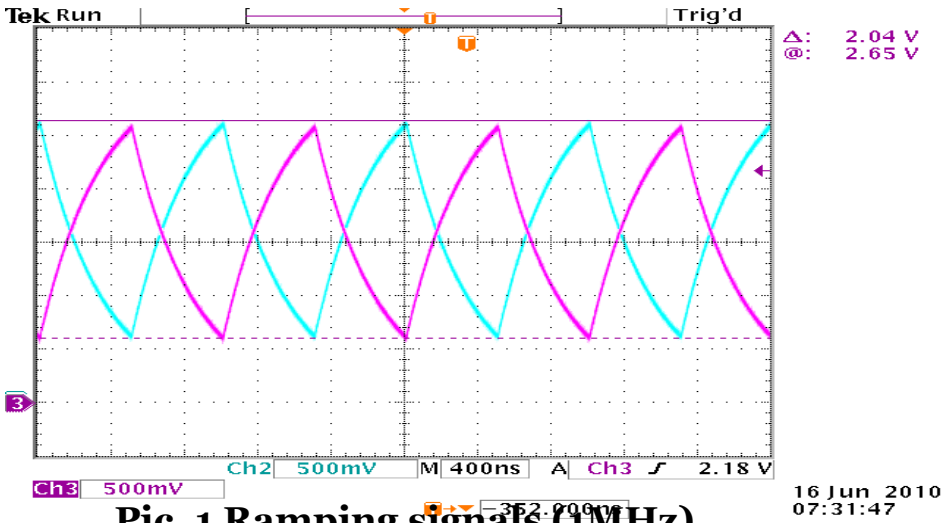


Performance Tests

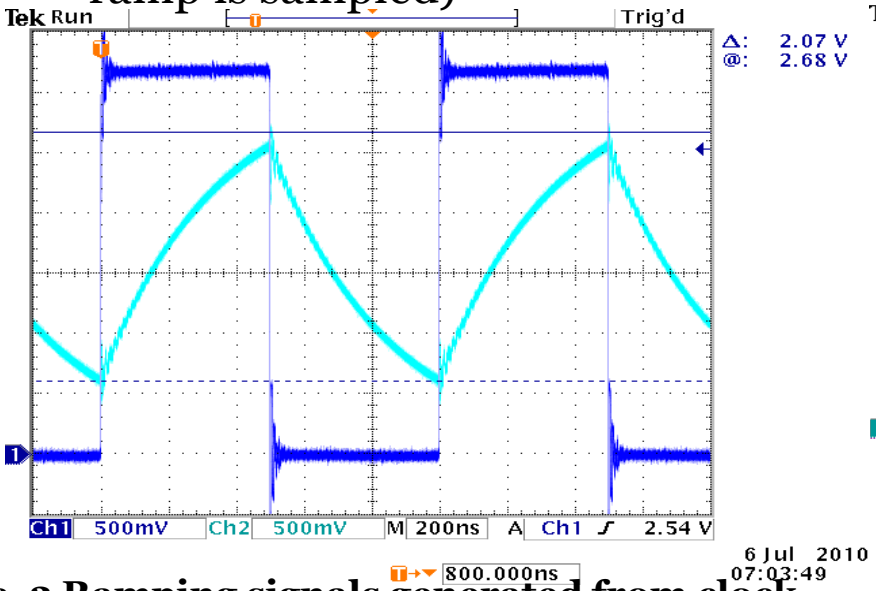
- Oscilloscope pictures
- Optimized range common mode signals
- Calibration
- Test Signals
- Histograms

Oscilloscope Pictures

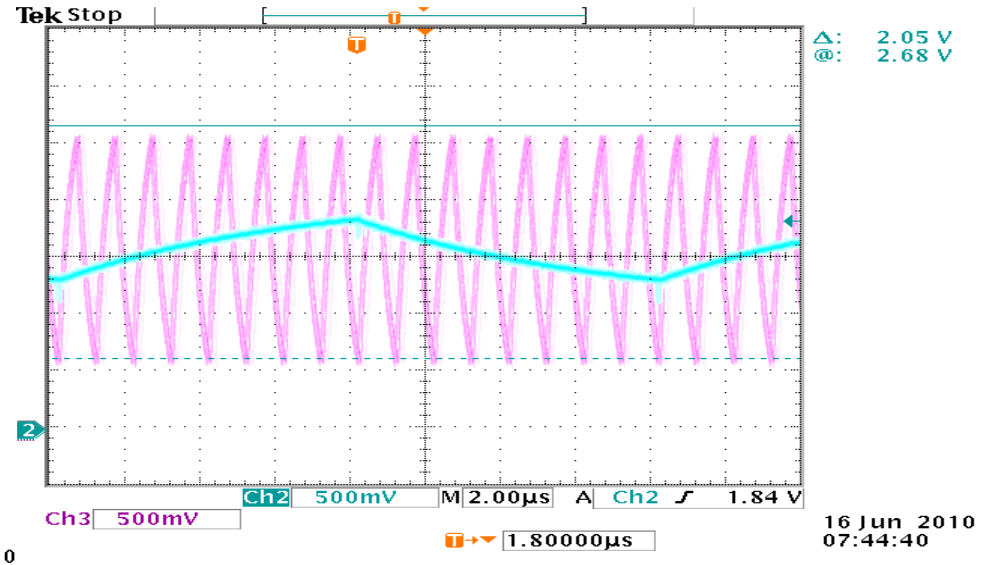
- Tests Start with analyzing critical signals
- Using a scope we can check the differential ramping signals.
- The ramping RC signals are derived from clocking signals in the board
- The ramping signal serves as a sampling signal (in pic. 3 a slower ramp is sampled)



Pic. 1 Ramping signals (1MHz)



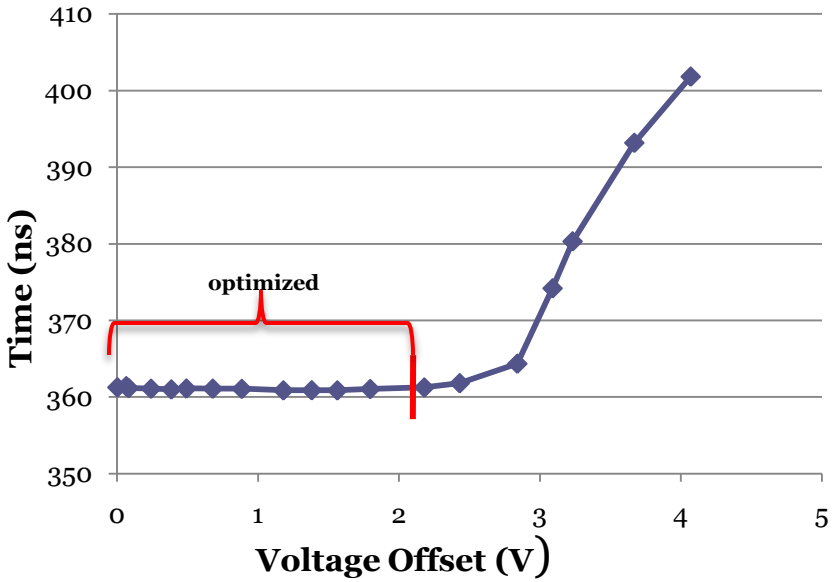
Pic. 2 Ramping signals generated from clock.

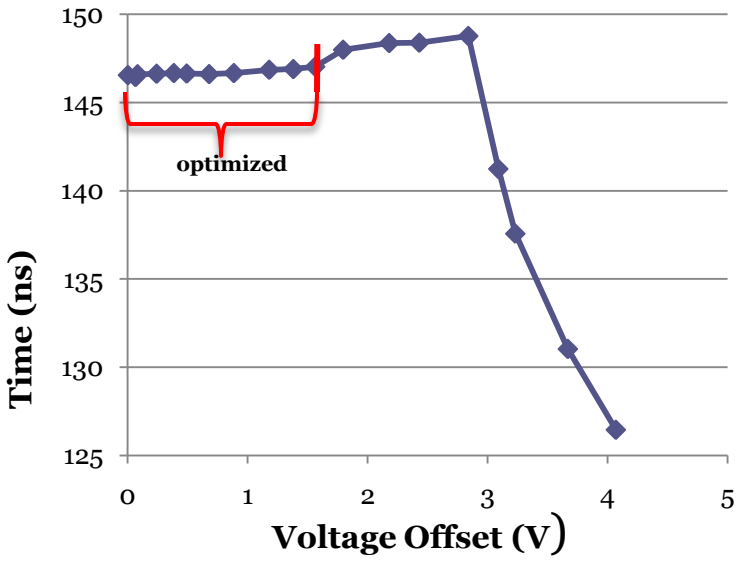


Pic. 3 Sampling using the ramping Signals

Common mode Signals

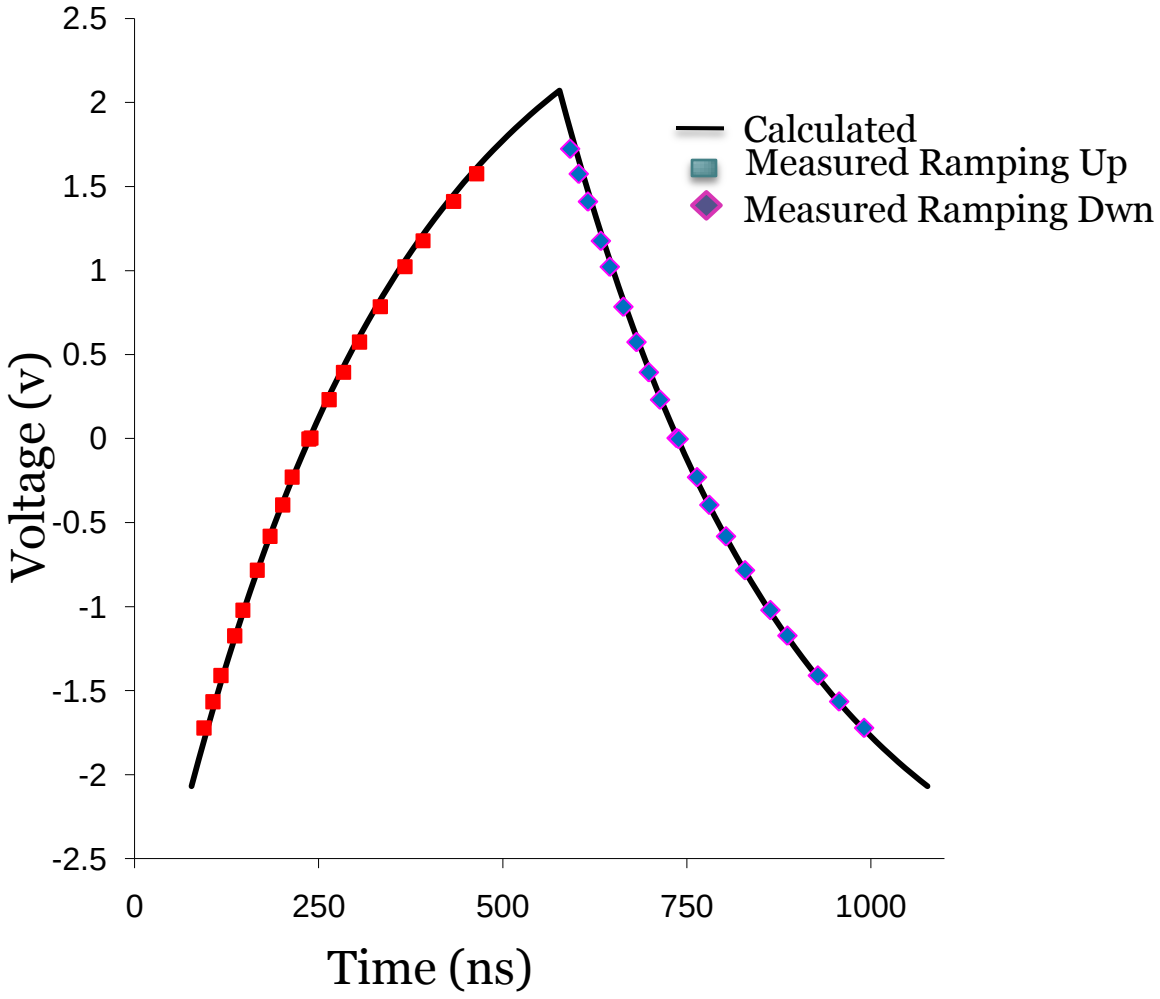
- Device is designed for differential Input Signals
- Performance can be compromised owing to offset of input signal.
- We can investigate this behavior by feeding common mode signals
- Observe that optimization is attained within the described range



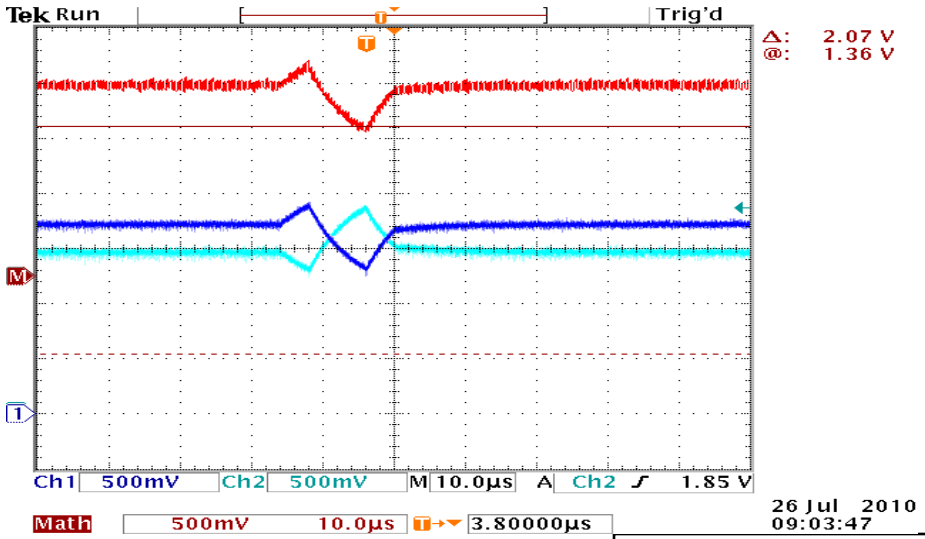


Calibration

- Check for accuracy of device by matching measured samples with calculated curve
- Generate a lookup table for time conversions
- Understand slight aberrations
- Moving forward in data interpretation

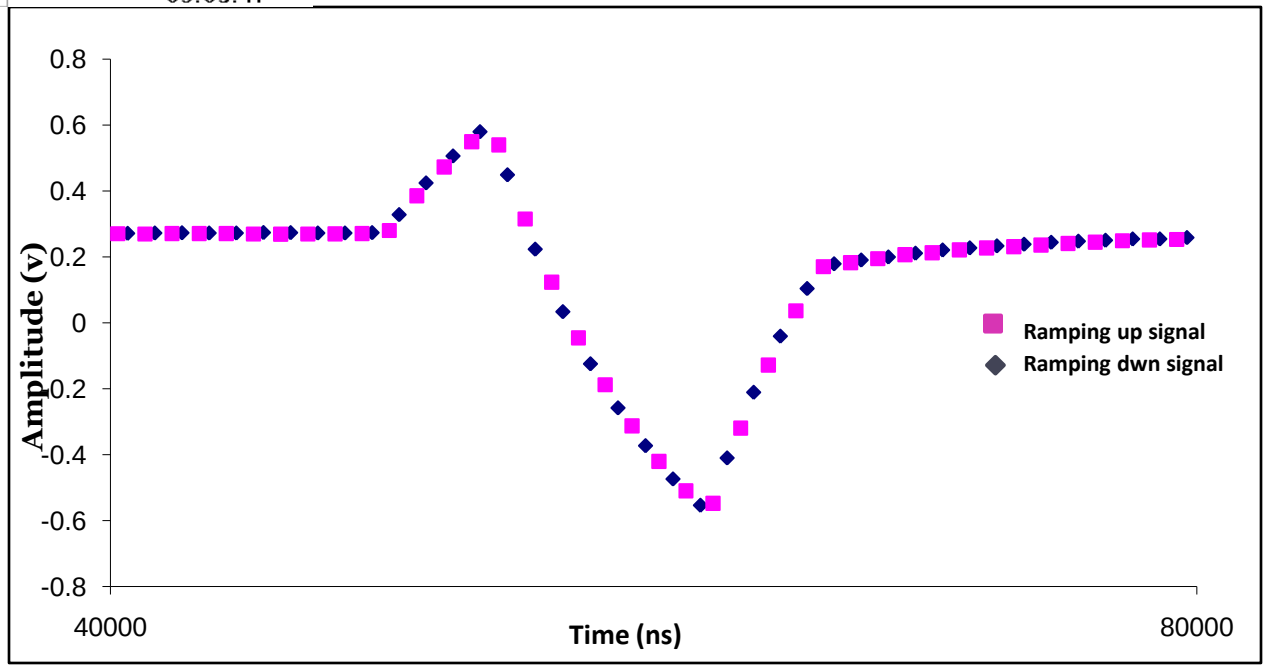


Test Signal



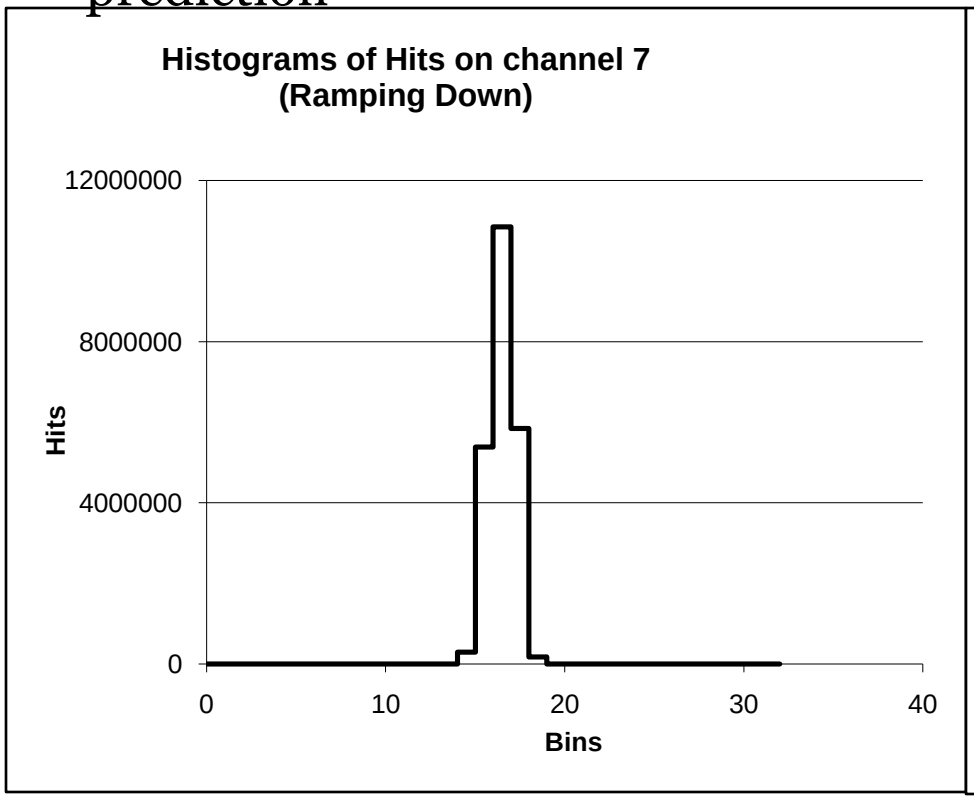
- A pulse signal is fed to an input channel
- Controlling the TDC through a serial port, the signal is sampled
- Raw data from the sampling is saved to a remote computer
- The goal is to recreate the signal using the array of hit time sampled

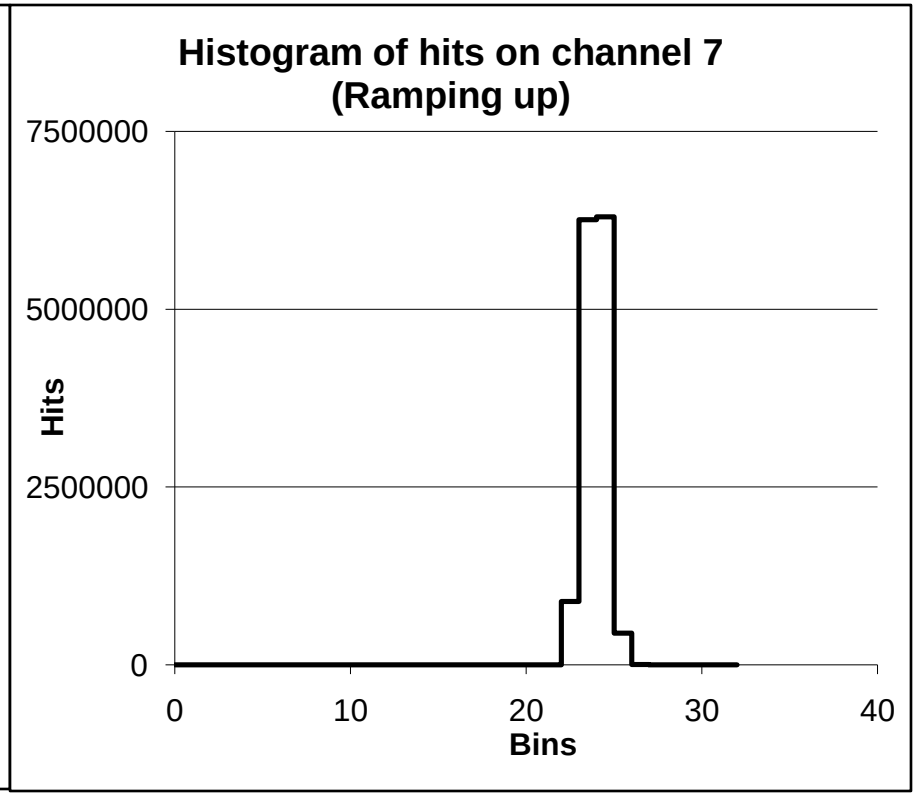
- With the calibration formula obtained we can regenerate input signals
- Ramping up and ramping down samples are converted and plotted in the same graph
- Notice that both signal samples match



Histograms

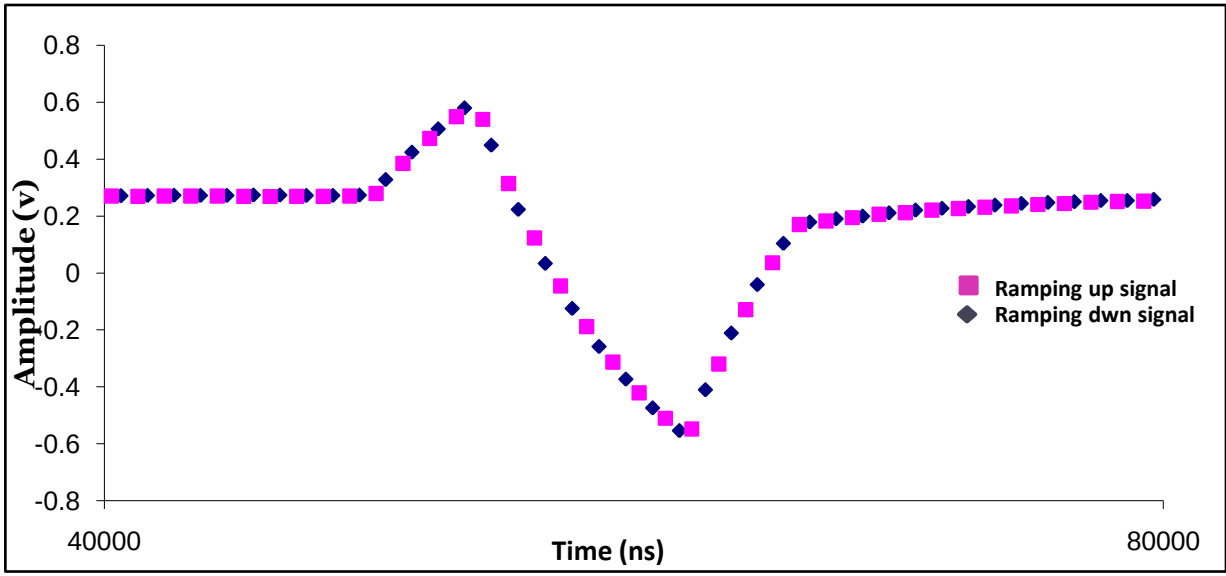
- Histograms plot bins on the LSB of Hit Time
- It's a pictorial evaluation of precision of the TDC.
- With a constant amplitude signal, we expect a sharp pic and little variance
- Channel 7 is supplied with a constant amplitude signal.
- Histograms of both ramping up and ramping down samples confirms our prediction

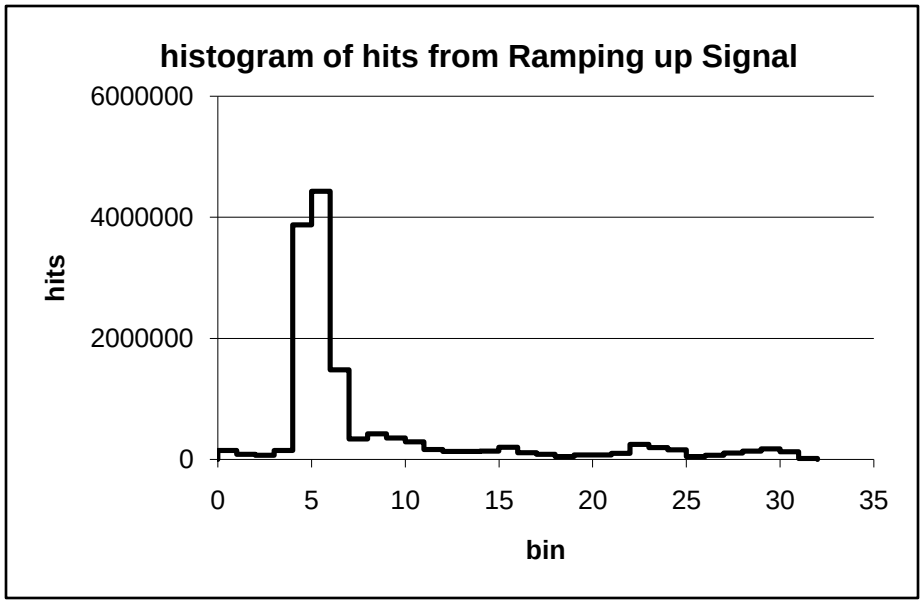


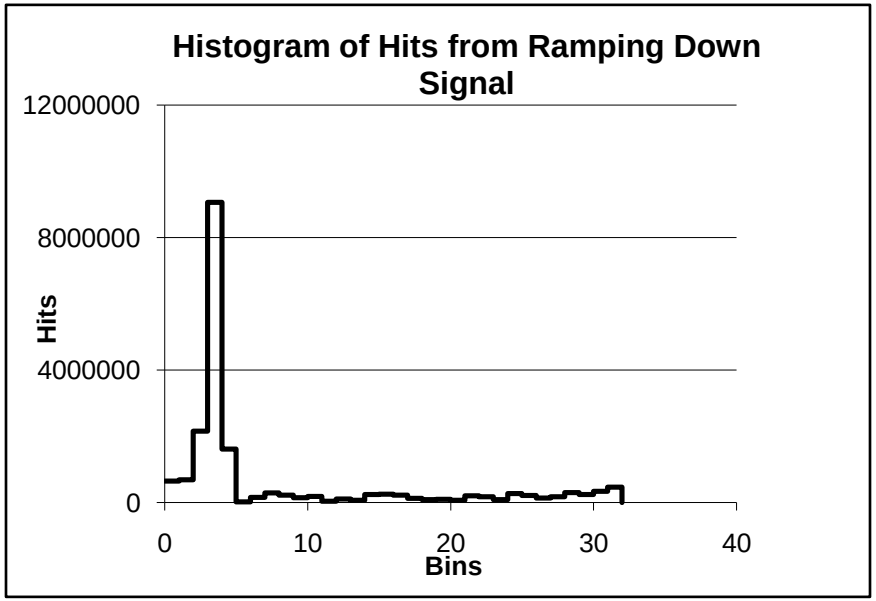


Histograms

- A varying amplitude like the pulse signal will be interesting to analyze on a histogram.
- Observe the noticeable peak and the smaller bumps.







Questions ??